FLIP-CHIP Market and Technology Trends

2013 Business Update

Flip Chip platform is still in mutation and provides continuously innovative fine pitch bumping solutions to serve the most advanced packaging technologies like 3DIC and 2.5D Interposer!
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- Methodology
- 2012 installed capacities
- Recent activity and investments for FC
- Focus on PTI’s recent investment
- Matching 2012 top down and bottom up
- Summary

### Flip-Chip market value

- Flip-Chip Market Value Forecast
- 2012 total Flip-Chip Market Value by COO segment
- 2012 total Flip-Chip Market Value by end use type
- 2012 Flip-Chip in package Market Value by COO segment
- 2018 total Flip-Chip Market Value by COO segment (forecast)

### Infrastructure & supply chain

- Transforming global IC Packaging Supply Chain*
- Flip-Chip Supply Chain
- Typical Flip Chip Flow-Chart
- Flip Chip Supply Chain Ecosystem
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- Business cases and supply chain examples
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2013 business update including µ-bumping!

…and many more new features…

“Flip-Chip 2011” report was the first Yole’s report dedicated to the flip-chip platform, its related bumping technologies and applications.

• This 2013 version provides an update of all the major parts describing this advanced packaging technological platform (market forecast, supply chain, technology trends and applications).

• Major changes and improvements
  – The new Yole’s top down approach has been used, leading to an exhaustive quantification of IC devices using flip-chip (80 IC screened, in 90 end products and 9 markets) leading to a more accurate modeling of the flip-chip market.
  – In the frame of this new top down approach, major changes and improvements have to be highlighted:
    • Flip-Chip micro-bumping has been included in this update to point out the impact of the brand new technological platforms (3DIC, 2.5D Interposer) driving new demand of FC copper pillar.
    • Accurate modeling of memory and HB-LED applications.
Also new in this 2013 report…

Market analysis

- Fully updated 2010 – 2018 market forecast
- Fully updated bottom up approach
  - 2012 installed capacities
  - 2010 – 2014 capacity expansion overview

Technology analysis

- Comparison between C2 and TCB
- Strong focus on micro-bumping for 3DIC & 2.5D
- Updated and new parts on assembly
  - TIM (new)
  - Flip-chip bonders (new)
  - Underfills
  - Substrates

Applications

- Flip-chip for HB-LED
- Micro-bumping in 3DIC and 2.5D Interposer applications
- Flip-chip for memories
- Flip-chip for analog, RF, mixed signals IC
What we highlighted, what we missed

in our 2011 Flip-Chip report

2011 Flip-Chip was the first Yole’s report on Flip-Chip technology, thus completing our report collection describing wafer level packaging infrastructure

• What we chose not to address
  – Thermal Interface Materials
  – Silicon to silicon Micro-bumping – but we mentioned it would be included in this new release
  – High Power LEDs since it was an emerging market with specific technologies

→ these 3 topics have been included in this new report

• What we missed
  – Flip-Chip adoption for memory, faster than expected

• What we highlighted / we pointed out
  – Our CAGR, wafer forecast, unit forecast and revenues forecast have been in good agreement with 2011/2012 production
  – We expected a wide adoption of Cu pillar for APE, BB and advanced CMOS ICs
  – We mentioned that Copper Pillar Bumping was on its way to become the next standard solution for flip chip bumping
  – Moreover, we concluded that “by largely contributing to the consolidation of the “middle-end” wafer level packaging infrastructure, flip chip will favor the fast growth of 3D wafer level packaging with through silicon vias (which require a similar infrastructure) and will benefit from it in return (fast growth of silicon to silicon micro-bumping, emergence of silicon and glass interposers in flip chip packages)”
Wafer Bumping Packaging and Applications

**Definition**

**WAFER BUMPING**

- **FLIP CHIP**
  - FC BGA
  - FC CSP
  - Chip on Board COF/COG
  - Silicon on silicon micro-bumping

  **Bump characteristics**
  - Plating, screen printing
  - Pitch: < 180µm

  **Bump characteristics**
  - Plating, screen printing, stud
  - Pitch: < 150µm

- **WAFER LEVEL PACKAGING**
  - **FAN IN**
  - **FAN OUT**
  - **CHIP EMBEDDING**

  **Bump characteristics**
  - Ball dropping
  - Pitch: 400-500µm

  **Bump characteristics**
  - Plating
  - Pitch: < 60µm

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**Scope of the 2013 Flip-Chip report**

- Courtesy of Statschippac
- Courtesy of 3M
- Courtesy of SPIL
- Courtesy of NXP and FCI
- Scope of the 2012 WLCSP report
- Scope of the 2012 fan-out/embedded report

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The objectives of this report are

- To update the business status of the Flip-Chip market
- To provide a forecast for the next five years, and predict future trends
- To provide an overview of the technological trends and applications that use Flip-Chip technology

The Flip-Chip market is studied from the following angles

- Market forecast (demand, production and installed capabilities)
- Industrial supply chain
- Market drivers
- Market value
- State-of-the-art technology and trends
- End-user applications
Company cited in the report

In 2012…

- Flip-Chip was a $20B market
- 20 M units ICs have been bumped (12.8M 12”eq wafers)
- Average fab loading rate was 78%
- Taiwan became the leading place for flip-chip bumping
- 50% of bumped wafers were used in a laptop or a desktop
- IC which are flip-chip packaged can be classified in 2 categories
  - Early adopters like GPU, CPU and Chipset that have been using FC for a long time
  - New comers like interposer IC, memory, APE, BB, that are moving fast to flip chip mainly motivated by the ultra fine pitch, the high IO count possibility and the provided performance of this interconnection solution
Flip-Chip drivers and benefits

Drivers and benefits provided by Flip-Chip

- High I/O density
- Large die-to-package fan-out area
- Interconnection to fine-pitch substrate
  - APE, BB in fcCSP
  - GPUs, CPUs, chipsets in fcBGA
  - Display drivers in COG, COF

- Electrical performance / interface bandwidth
  - In particular for APE, GPUs, FPGAs, ASICs, PMU, RF Tx, memories

- Thermal dissipation
  - CPUs, GPUs, PA

- Hermeticity
  - SAW filters

- Ergonomics, topology
  - CMOS Image Sensors and LEDs
Flip-Chip wafer forecast by bumping metallurgy

Flip-chip bumping wafer forecast*
Breakdown by bumping metallurgy (12'' eq wafers)

Yole Developpement © February 2013

2010 – 2018 Flip-Chip CAGR = 19%

*3D µ-bumping included

- Cu Pillar
- Lead Free Solder
- Sn/Pb Eutectic Solder
- Gold Stud + Plated
• Cu Pillar is already a well established platform, especially due to Intel that started Cu pillar bumping of processors in 2006

• This technology diffused during the 7 last years within the industry and today, the important expected growth of Cu pillar bumping (35% CAGR on the 2010 – 2018 time frame) is mainly linked to the big demand coming from 3 areas
  – CMOS 28nm IC (and beyond), including new types of ICs like Application Processors (APE), Base Band module (BB) for mobile phones
  – Next generation of DDR Memories (DDR3 and DDR4 memories)
  – 3DIC/2.5D Interposer using Cu pillar (μbumping)

• μbumping for 3DIC and 2.5D Interposer is a real game changer for the packaging industry and we decided to include it in our updated market forecast to highlight how it will impact the flip-chip landscape
In 2012, Laptop and desktop PC were the top end products using Flip Chip

PCs are followed by Smart TV and LCD TVs (for LCD drivers), smartphones and high performance computers
Wafer Bumping Trends

Pitch capabilities / Alloy

Bumping interconnect technology roadmap for FC BGA

- **Screen Printing**
  - solder bump
  - conductive polymer bump

- **Electroplating / Evaporation / Stud bumping**
  - Au bump
  - Solder bump
  - Cu-pillars

- **Electroplating**
  - Cu-Pillars
  - μ-Bumps

- **Micro-bump bonding**

- **Bump-less ‘pads’?**

- **2002 - 2019**

- **Eutectic, High Lead, Pb free (SnAgCu)**

- **Lead free, Au stud, Solder bump, Cu pillars**
Bumping Hierarchy* in Flip Chip
& related 3D Packaging Solutions as of 2013

μ-Bumps: 10-40µm

Wide I/O memory stack

µ-Bumps 20-80µm

2.5D Silicon interposer

Bumps/Cu Pillars: 40-250µm

BGA Laminate

400-800µm

PCB

• μ-bumping for 2.5D & 3DIC in conjunction with new applications like APE, DDR memories etc. is going to boost flip-chip demand, thus leading also to new challenges and new technological developments. Today flip-chip is available through a wide range of pitches to answer specific needs of all the applications:
  - μ-bumping for advanced 3D stacking: 10 – 20 µm pitch required
  - CMOS 28nm and below, logic on interposer etc.: 20 – 80 µm pitch required
  - Other logic (in FC BGA): 40 – 450 µm pitch required
Flip-Chip technology is already present in a wide range of application, from high volumes/consumer applications, to low volumes/high end applications. All these applications have their own requirements, specifications and challenges!
Lionel Cadix

- Lionel joined Yole after completing several projects linked to the characterization and modeling of high-density TSV and 3DIC chip stacking in collaboration with CEA-Leti and STMicroelectronics for his PhD. He is the author of several publications and holds eight patents in the field of 3D Integration.

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